

Description

JMT P-channel Enhancement Mode Power MOSFET

Features

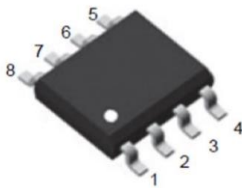
- -40V, -6A
 $R_{DS(ON)} < 38m\Omega @ V_{GS} = -10V$
 $R_{DS(ON)} < 46m\Omega @ V_{GS} = -4.5V$
- Advanced Trench Technology
- Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead Free

Applications

- Load Switch
- PWM Application
- Power Management



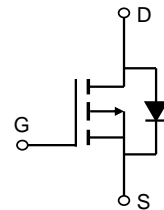
100% UIS TESTED!
100% ΔVds TESTED!



SOP-8 Top View



Marking and Pin Assignment



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Outline	Package	Reel Size	Reel(pcs)	Per Carton (pcs)
440P04A	JMTP440P04A	TAPING	SOP-8	13"	4000	48000

Absolute Maximum Ratings (@ $T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Value	Units
V_{DS}	Drain-to-Source Voltage	-40	V
V_{GS}	Gate-to-Source Voltage	± 20	V
I_D	Continuous Drain Current	$T_A = 25^\circ\text{C}$	-6
		$T_A = 100^\circ\text{C}$	-4
I_{DM}	Pulsed Drain Current ⁽¹⁾	-24	A
E_{AS}	Single Pulsed Avalanche Energy ⁽²⁾	25	mJ
P_D	Power Dissipation	$T_A = 25^\circ\text{C}$	1.7
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient ⁽³⁾	76	$^\circ\text{C}/\text{W}$
T_J, T_{STG}	Junction & Storage Temperature Range	-55 to 150	$^\circ\text{C}$



Electrical Characteristics (T_J = 25°C unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	I _D = -250μA, V _{GS} = 0V	-40	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -40V, V _{GS} = 0V	-	-	-1.0	μA
I _{GSS}	Gate-Body Leakage Current	V _{DS} = 0V, V _{GS} = ±20V	-	-	±100	nA
On Characteristics						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = -250μA	-1.0	-1.7	-2.5	V
R _{DS(ON)}	Static Drain-Source ON-Resistance ⁽⁴⁾	V _{GS} = -10V, I _D = -6A	-	29	38	mΩ
		V _{GS} = -4.5V, I _D = -4A	-	35	46	mΩ
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{GS} = 0V, V _{DS} = -20V, f = 1MHz	-	1244	-	pF
C _{oss}	Output Capacitance		-	97	-	pF
C _{rss}	Reverse Transfer Capacitance		-	80	-	pF
Q _g	Total Gate Charge	V _{GS} = 0 to -10V V _{DS} = -20V, I _D = -5A	-	23	-	nC
Q _{gs}	Gate Source Charge		-	4	-	nC
Q _{gd}	Gate Drain("Miller") Charge		-	4	-	nC
Switching Characteristics						
t _{d(on)}	Turn-On Delay Time	V _{GS} = -10V, V _{DD} = -20V I _D = -5A, R _{GEN} = 3Ω	-	5	-	ns
t _r	Turn-On Rise Time		-	2	-	ns
t _{d(off)}	Turn-Off Delay Time		-	51	-	ns
t _f	Turn-Off Fall Time		-	29	-	ns
Drain-Source Diode Characteristics and Max Ratings						
I _S	Maximum Continuous Drain to Source Diode Forward Current		-	-	-6	A
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	-24	A
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0V, I _S = -6A	-	-	-1.2	V
t _{rr}	Body Diode Reverse Recovery Time	I _F = -5A, di/dt = 100A/us	-	13	-	ns
Q _{rr}	Body Diode Reverse Recovery Charge		-	7	-	nC

- Notes:
1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.
 2. E_{AS} condition: Starting T_J=25C, V_{DD}=-20V, V_G=-10V, R_G=25ohm, L=0.5mH, I_{AS}=-10A
 3. R_{θJA} is measured with the device mounted on a 1inch² pad of 2oz copper FR4 PCB
 4. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 0.5%.

Typical Performance Characteristics

Figure 1: Output Characteristics

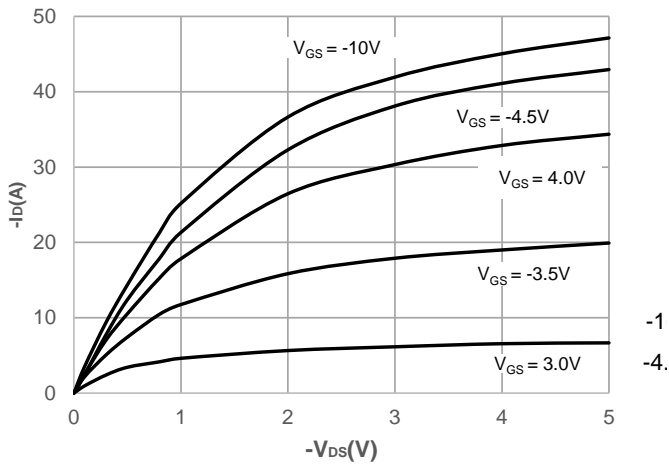


Figure 2: Typical Transfer Characteristics

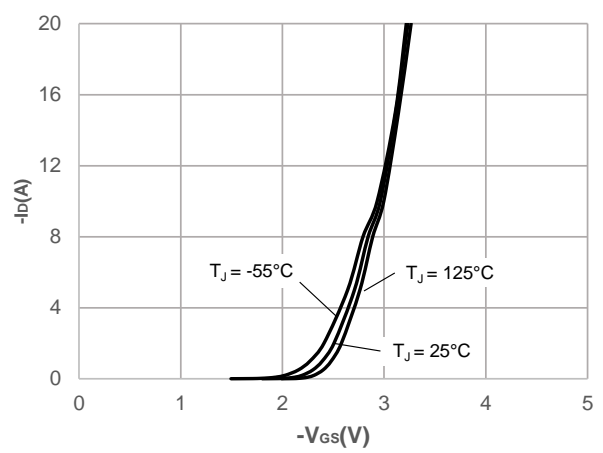


Figure 3: On-resistance vs. Drain Current

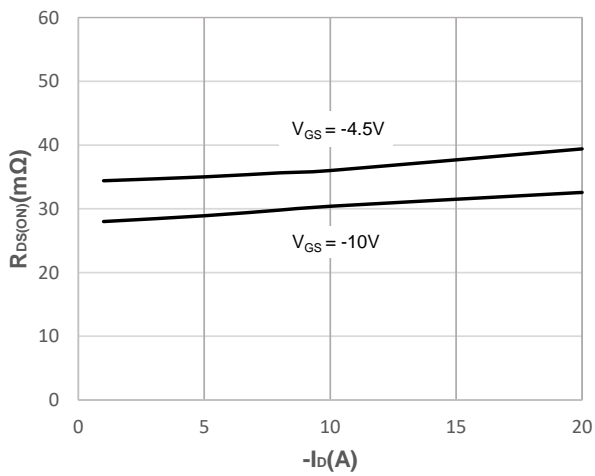


Figure 4: Body Diode Characteristics

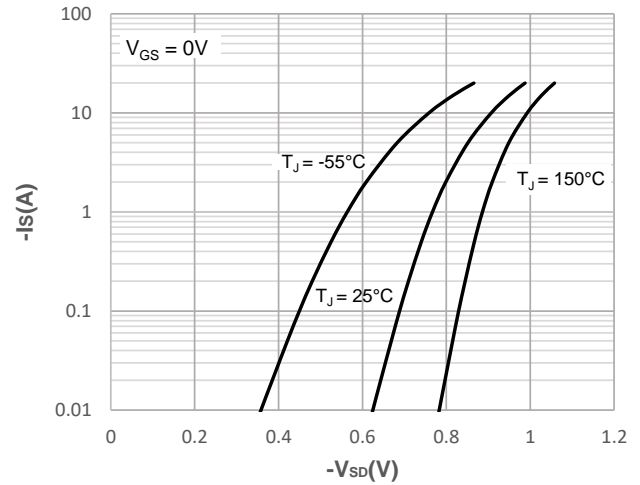


Figure 5: Gate Charge Characteristics

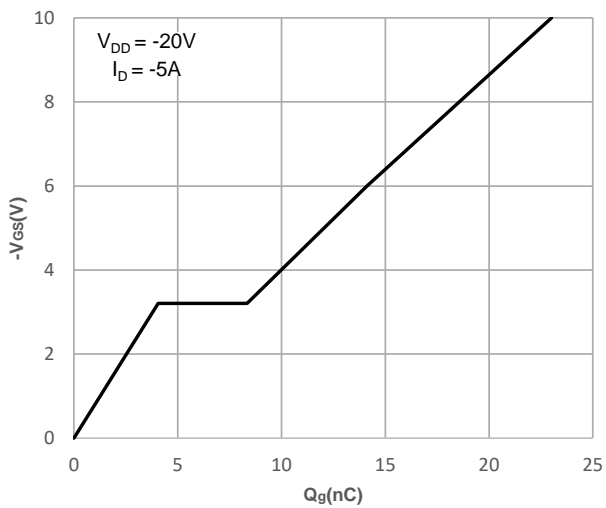
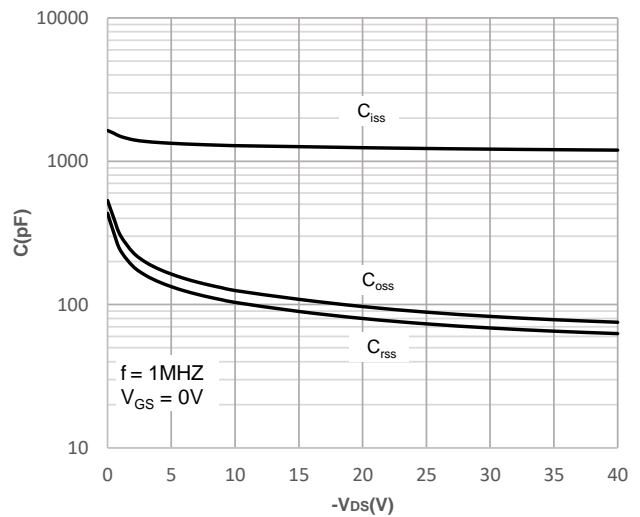


Figure 6: Capacitance Characteristics



Typical Performance Characteristics

Figure 7: Normalized Breakdown voltage vs. Junction Temperature

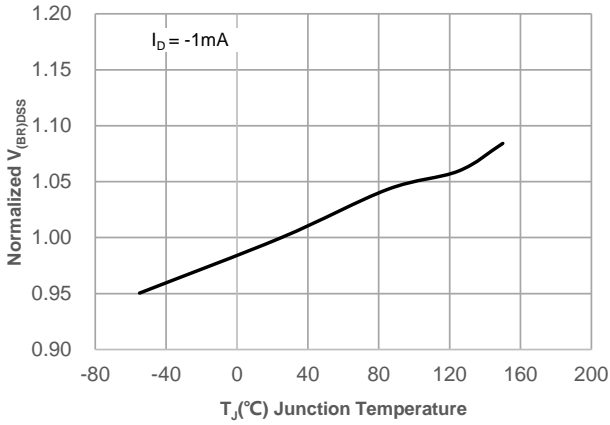


Figure 8: Normalized on Resistance vs. Junction Temperature

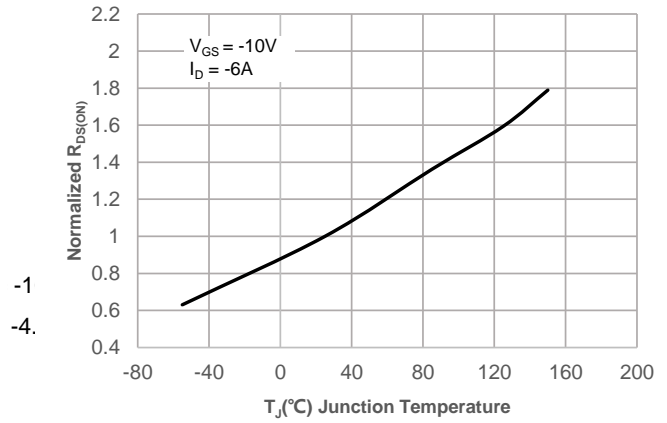


Figure 9: Maximum Safe Operating Area

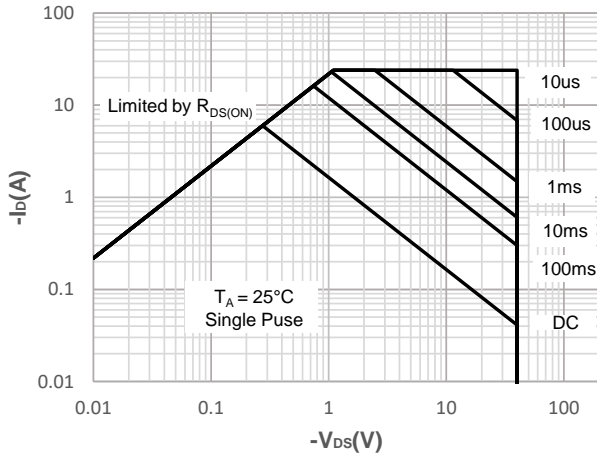


Figure 10: Maximum Continuous Driand Current vs. Ambient Temperature

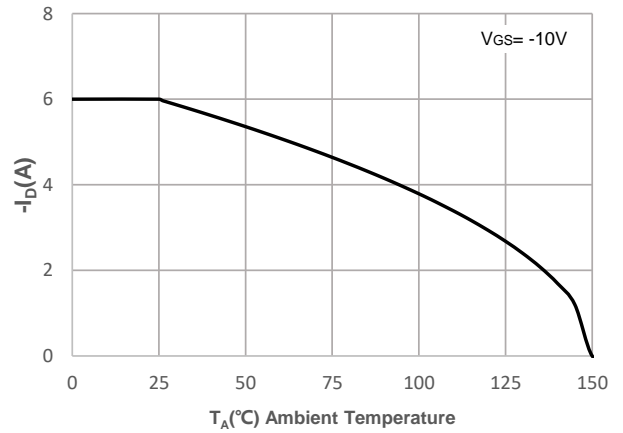


Figure 11: Normalized Maximum Transient Thermal Impedance

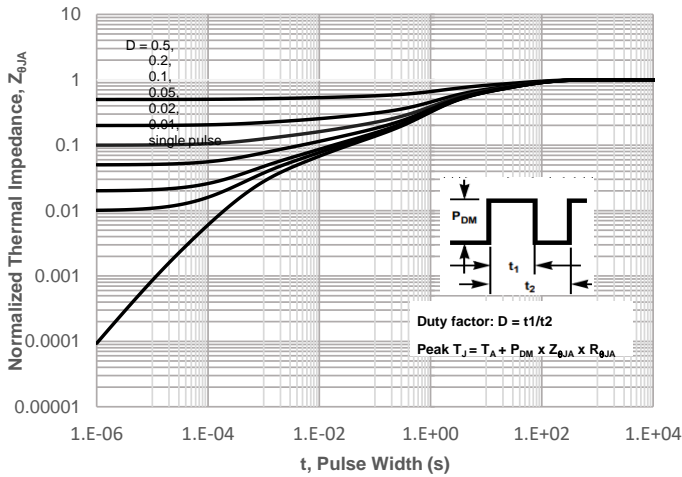
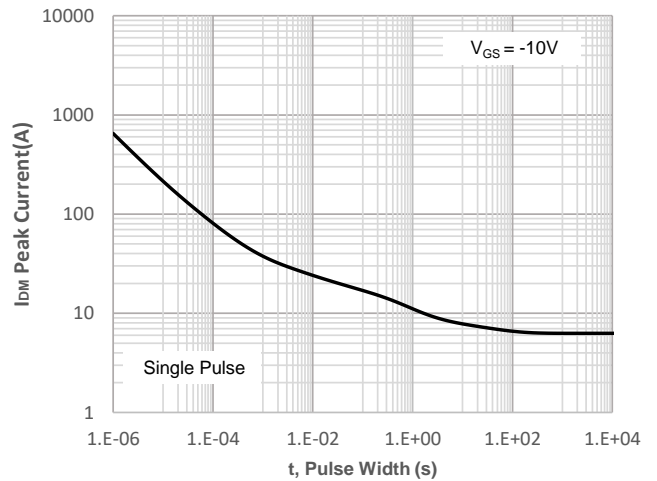


Figure 12: Peak Current Capacity



Test Circuit

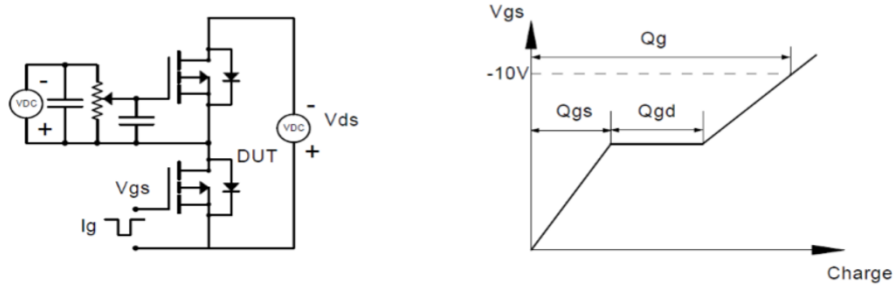


Figure 1: Gate Charge Test Circuit & Waveform

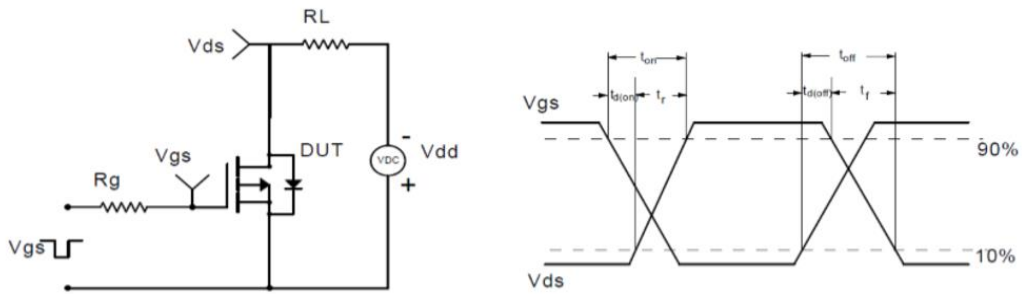


Figure 2: Resistive Switching Test Circuit & Waveform

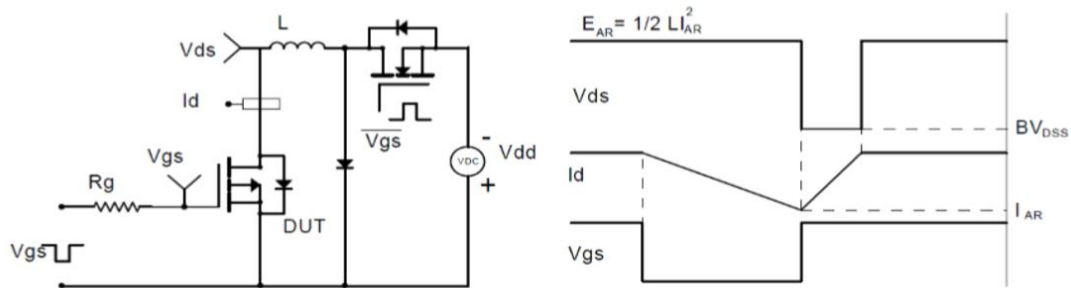


Figure 3: Unclamped Inductive Switching Test Circuit & Waveform

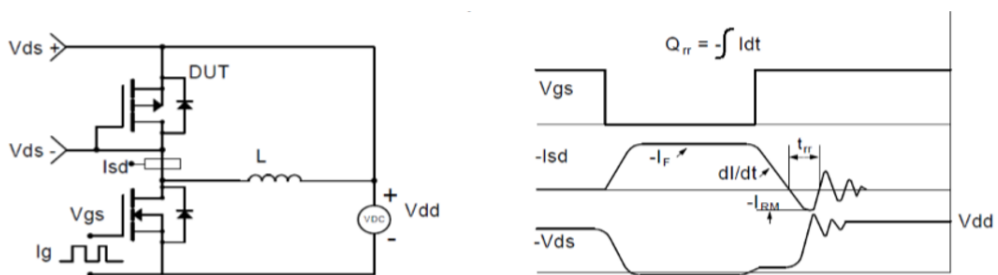
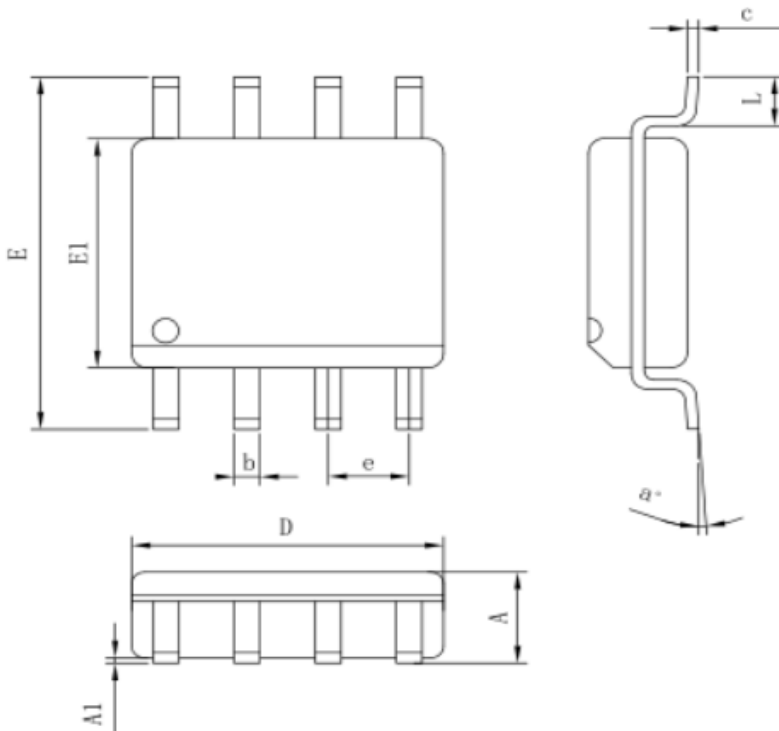



Figure 4: Diode Recovery Test Circuit & Waveform

Package Mechanical Data(SOP-8)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	--	--	1.75
A1	0.10	--	0.23
b	0.35	--	0.48
c	0.19	--	0.25
D	4.70	4.90	5.00
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27BSC		
L	0.50	--	0.80
a*	0*	--	8*

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